Helmholtz Call for 2017 CSC Fellowship Applicants

Helmholtz Centre: Forschungszentrum Juelich GmbH – www.fz-juelich.de

Department/Institute: Peter Grünberg Institute, Semiconductor Nanoelectronics (PGI-9)
http://www.fz-juelich.de/pgi/pgi-9/EN/Home/home_node.html

Supervising scientist: Prof. Dr.Siegfried Mantl/Prof. Dr. Qing-Tai Zhao

University for Registration (for those looking for a dissertation) : RWTH Aachen

Research Field: Key Technology/ Nanometer semiconductor devices

Position: PhD Student **or** Sandwich PhD Student

Research Area:

Power consumption is the grand challenge in semiconductor industry. For MOSFETs the reduction of the supply voltage V_{dd} is hindered by the physical thermal limit of the subthreshold swing $SS = m \times 60mV/dec \geq 60mV/dec$ at 300K. On the base of thermal emission, the dominating transport mechanism of a MOSFET, SS<60mV/dec at 300K can only be achieved when the body factor $m < 1$. This can be done by replacing the gate insulator with a ferroelectric layer, forming a negative capacitance FET (NCFET).

In this project we will investigate NCFET with HfO2 based ferroelectric materials. Integration of ferroelectric layer with planar and nanowire MOSFETs to form NCFET will be studied to achieve SS<60mV/dec at room temperature.

All these tasks require extensive process investigations, structural and electrical characterization of nanowires and the production of test structures and transistors. A fully equipped clean room, various epitaxy and deposition tools as well as numerous analysis methods are available.

A successful PhD-thesis may be defended at the university RWTH Aachen.

Specific Requirements:

-Excellent knowledge of solid state physics and possibly device physics;
-The ability to work and communicate within a scientific team in fluent English.

Duration of stay: 2 years (Sandwich PhD); 4 years (PhD)

Work Place: Forschungszentrum Juelich, Germany (near Cologne)

Earliest Start: September 2017

Language Requirement: very good English language (writing and speaking)

Name and Address of the Supervisor: Dr. Qing-Tai Zhao, Forschungszentrum Juelich, Peter Grünberg Institute (PGI 9-IT), 52425 Juelich, Germany
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Research Area:

Power consumption is the grand challenge in semiconductor industry. Steep slope transistors, like band-to-band tunnelling field effect transistors (TFETs), which beat the thermal transport limitation of MOSFETs with a minimum inverse subthreshold slope *SS* of 60 mV/dec at room temperature, are required for a reduction of the supply voltage V_{dd} to lower the power consumption. TFETs face the challenges of high on-currents and small average SS<60mV/dec. Tunnelling is enhanced for smaller band gap materials such as strained Si, SiGe, Ge and GeSn in comparison to Si. TFETs further benefit from good electrostatic control, which can be improved by employing multi-gate nanowire structures. New concepts with vertical tunnelling are also employed to improve the device performance.
The objective of this project is to realize TFETs with high on-currents and very steep slopes (<60mV/dec over 2-4 orders of magnitude drain currents). Nanowire and heterostructure TFETs will be fabricated and characterized based on group IV semiconductors. The tunnelling junctions and high-k/metal gate stacks will be optimized. Electron beam lithography is used to pattern the nanowires.

All these tasks require extensive process investigations, structural and electrical characterization of nanowires and heterostructures and the production of test transistors. A fully equipped clean room, various epitaxy and deposition tools as well as numerous analysis methods are available.

Specific Requirements:

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